



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

09/905,511

07/13/2001

Gyudong Kim

19570-06205

3384

7590

06/14/2005

Paul L. Hickman  
Patent Attorney  
Perkins COIE LLP  
P.O. Box 2168  
Menlo Park, CA 94026-2168

EXAMINER

WILLIAMS, LAWRENCE B

ART UNIT

PAPER NUMBER

2638

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/905,511

Applicant(s)

KIM ET AL.

Examiner

Lawrence B. Williams

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 14 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-51 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 44-47 and 51 is/are allowed.
- 6) ☒ Claim(s) 1-43 and 48 is/are rejected.
- 7) ☒ Claim(s) 49 and 50 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### *Claim Objections*

1. Claims 31, 32 are objected to because of the following informalities: Examiner suggest applicant correct the spelling of claim in line 1 of both claims.

Appropriate correction is required.

2. The indicated allowability of claims 34-38 is withdrawn in view of the newly discovered reference(s) to Nagaraj et al. (US Patent 5,208,546) and Dong (US Patent 5,268,655). Rejections based on the newly cited reference(s) follow.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3-5, 7-8, 34, 36, 38-39, 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent 5,828,255) in view of Dong (US Patent 5,268,655).

(1) With regard to claim 1, Kelkar et al. discloses in Figs. 4-6, a method of reducing jitter

Art Unit: 2634

in data transmission between a transmitter and a receiver, where the receiver has a phase-locked loop (PLL) (701) with a loop bandwidth for recovering the clock and data from the transmitter, the method comprising the steps of: measuring relative jitter (703) between the recovered clock and the recovered data at the receiver and adaptively adjusting the PLL loop bandwidth of the receiver to reduce the relative jitter (abstract; col. 9, line 60 - col. 10, line 14). Kelkar et al. does not however disclose measuring phase pointer activity where the phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver, wherein the phase pointer activity is measured as the absolute sum of the directional changes of the phase pointer.

However, Dong discloses measuring phase pointer activity where the phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver, wherein the phase pointer activity is measured as the absolute sum of the directional changes of the phase pointer (col. 2, lines 32-46).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Dong into the invention of Kelkar et al. as a method of providing a self-adjusting PLL to reduce jitter (col. 1, lines 51-60).

(2) With regard to claim 3, claim 3 inherits all limitations of claim 1. Furthermore, though Kelkar et al does not explicitly disclose the PLL for generating both the clock and the data, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating both the clock and data.

(3) With regard to claim 4, claim 4 inherits all limitations of claim 1. Furthermore, though Kelkar et al. does not explicitly disclose the PLL for generating both the clock and the

data, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating both the data.

(4) With regard to claim 5, claim 5 inherits all limitations of claim 1 above.

(5) With regard to claim 7, claim 7 inherits all limitations of claim 5. Furthermore, though Kelkar et al. does not explicitly disclose the PLL for generating both the clock and the data, he does teach his invention for PLLs having different applications, which would inherently include a PLL for generating both the clock and data.

(6) With regard to claim 8, claim 8 inherits all limitations of claim 5. Furthermore, though Kelkar et al. does not explicitly disclose the PLL for generating both the clock and the data, he does teach his invention for PLLs having different applications, which would inherently include a PLL for generating both the clock and data.

(7) With regard to claim 34, claim 34 inherits all limitations of claim 5 above.

(8) With regard to claim 36, claim 36 inherits all limitations of claim 34 above.

Furthermore, Dong discloses wherein the phase pointer activity is measured as the absolute sum of the directional changes of the phase pointer (col. 2, lines 32-46).

(9) With regard to claim 37, claim 37 inherits all limitations of claim 34 above.

Furthermore, Kelkar et al. also discloses wherein the pointer activity is measured as the frequency of the changes of the phase pointer (col. 7, line 63 - col. 8, line 32).

(10) With regard to claim 38, claim 38 inherits all limitations of claim 34 above. Though both inventors are silent as to the type of encoding scheme used, it would be obvious to one skilled in the art that the type of encoding would be irrelevant since both inventions are geared toward the measurement of jitter and removal thereof.

(11) With regard to claim 39, claim 39 inherits all limitations of claim 1 above.

(12) With regard to claim 42, claim 42 inherits all limitations of claim 39 above.

Furthermore, Dong also discloses the step of determining a local minimum if the difference is below a threshold (col. 5, lines 14-40).

(13) With regard to claim 48, Dong et al. also discloses measuring an error, and adaptively adjusting the PLL loop bandwidth to reduce the error rate (abstract).

5. Claims 2, 6, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent 5,828,255) in view of Dong (US Patent 5,268,655) as applied to claims 1, 5 and 34 above, and further in view of Ahn et al. (US 2002/0064247 A1).

(1) With regard to claim 2, claim 2 inherits all limitations of claim 1 above. As noted above, Kelkar et al in combination with Dong disclose all limitations of claim 1 above. The do not however disclose wherein the relative jitter is represented by the activity of a phase pointer indicating a correct data sampling point.

However, Ahn et al. discloses wherein the relative jitter is represented by the activity of a phase pointer indicating a correct data sampling point [0058].

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Ahn et al. with the teachings of Kelkar et al in combination with Dong as a method of reducing substantial distortion in a received signal [0007].

(2) With regard to claim 6, claim 6 inherits all limitations of claims 2 and 5 above.

(3) With regard to claim 35, claim 35 inherits all limitations of claims 2 and 34 above.

Art Unit: 2634

6. Claims 9, 10, 14-17, 19, 20, 26-27, 29, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent 5,828,255) in view of Dong (US Patent 5,268,655).

(1) With regard to claim 9, Kelkar et al. discloses in Figs. 4-6, a method of reducing jitter in data transmission between a transmitter and a receiver, where the receiver has a phase-locked loop (PLL) (701) with a loop bandwidth for recovering the clock and data from the transmitter. Kelkar et al. does not however disclose the method comprising the steps of: measuring phase pointer activity where the phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver, wherein the phase pointer is determined from integration of the magnitude of AC component of a control voltage representing the phase changes of the received data and adaptively adjusting a characteristic of the receiver so as to reduce the phase pointer activity.

However, Dong discloses measuring phase pointer activity where the phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver, wherein the phase pointer is determined from integration of the magnitude of AC component of a control voltage representing the phase changes of the received data and adaptively adjusting a characteristic of the receiver so as to reduce the phase pointer activity (col. 4, line 62- col. 5, line 40).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Dong with those of Kelkar et al. as a method of providing a self-adjusting PLL to reduce jitter (col. 1, lines 51-60).

(2) With regard to claim 10, Kelkar et al also discloses wherein the characteristic of the receiver includes the receiver PLL bandwidth (col. 9, line 60 – col. 10, line 14).

(3) With regard to claim 14, Dong also discloses wherein the phase pointer activity is measured as the absolute sum of the directional changes of the phase pointer (col. 2, lines 32-46).

(4) With regard to claim 15, Kelkar et al. also discloses wherein the pointer activity is measured as the frequency of the changes of the phase pointer (col. 7, line 63-col. 8, line 32).

(5) With regard to claim 16, claim 16 inherits all limitations of claim 9. Furthermore, though Kelkar et al does not explicitly disclose the PLL for generating both the clock and the data, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating both the clock and data.

(6) With regard to claim 17, claim 17 inherits all limitations of claim 19. Furthermore, though Kelkar et al. does not explicitly disclose the PLL for generating the data only, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating the data.

(7) With regard to claim 19, claim 19 inherits all limitations of claim 9 above.

(8) With regard to claim 20, claim 20 inherits all limitations of claim 19 above. Furthermore, Kelkar et al also discloses wherein the characteristic of the receiver includes the receiver PLL bandwidth (col. 9, line 60 – col. 10, line 14).

(9) With regard to claim 26, claim 26 inherits all limitations of claim 19. Furthermore, though Kelkar et al does not explicitly disclose the PLL for generating both the clock and the data, he does teach his invention for PLLs having different applications, which inherently would include a PLL for generating both the clock and data.

(10) With regard to claim 27, claim 27 inherits all limitations of claim 19. Furthermore, though Kelkar et al. does not explicitly disclose the PLL for generating only the data, he does



Art Unit: 2634

teach his invention for PLLs having different applications, which inherently would include a PLL for generating only the data.

(11) With regard to claim 29, claim 29 inherits all limitations of claim 9 above. Though both inventors are silent as to the type of encoding scheme used, it would be obvious to one skilled in the art that the type of encoding would be irrelevant since both inventions are geared toward the measurement of jitter and removal thereof.

(12) With regard to claim 32, claim 32 inherits all limitations of claim 29 above. Furthermore, Kelkar et al. also discloses wherein the pointer activity is measured as the frequency of the changes of the phase pointer (col. 7, line 63 - col. 8, line 32).

7. Claims 11-12, 21-22, 24, 25, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent 5,828,255) in view of Dong (US Patent 5,268,655) as applied to claims 9, 19 and 29 above, and further in view of Ahn et al. (US 2002/0064247 A1).

(1) With regard to claim 11, as noted above, Kelkar et al. in combination with Dong disclose all limitations of claim 9 above. They do not however explicitly disclose wherein the phase pointer is selected from oversampled points.

However Ahn et al. discloses in Fig. 1, wherein the phase pointer activity is selected from oversampled points.

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Ahn et al. with the teachings of Kelkar et al. in combination with Dong as a method of reducing substantial distortion in a received signal.

Art Unit: 2634

(2) With regard to claim 12, Ahn et al. also discloses wherein the phase pointer is determined from a digital tracking pointer representing the phase changes of the received data [0058-0059].

(3) With regard to claim 21, claim 21 inherits all limitations of claims 11 and 19 above.

(4) With regard to claim 22, claim 22 inherits all limitations of claims 12 and 19 above.

(5) With regard to claim 24, Dong also discloses wherein the phase pointer activity is measured as the absolute sum of the directional changes of the phase pointer (col. 2, lines 32-46).

(6) With regard to claim 25, claim 25 inherits all limitations of claim 19 above. Furthermore, Kelkar et al. also discloses wherein the pointer activity is measured as the frequency of the changes of the phase pointer (col. 7, line 63 - col. 8, line 32).

(7) With regard to claim 30, claim 30 inherits all limitations of claims 11 and 29 above.

(8) With regard to claim 31, claim 31 inherits all limitations of claim 29 above. Furthermore, Ahn et al. also discloses wherein the phase pointer is determined from a digital tracking pointer representing the phase changes of the received data [0058-0059].

8. Claims 18, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US Patent 5,828,255) in view of Dong (US Patent 5,268,655) as applied to claims 9, 19 above and further in view of Dinh (US Patent 6,038,276).

(1) With regard to claim 18, as noted above, Kelkar et al. in combination with Dong disclose all limitations of claim 9 above. They do not however disclose wherein the transmitter PLL bandwidth changes depending on a video mode.

Art Unit: 2634

However, Dinh discloses wherein the transmitter PLL bandwidth changes depending on a video mode (col. 13, lines 36-47).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dinh with the invention of Kelkar et al. in combination with Dong as a method of implementing an improved phase lock loop in digital and analog video environment (col. 2, line 63- col. 4, line 10).

(2) With regard to claim 28, claim 28 inherits all limitations of claim 19 and 18 above.

*Allowable Subject Matter*

9. Claims 44-47, 51 are allowed.

10. Claims 49, 50 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

The instant application discloses a method and apparatus for controlling the loop bandwidth of a PLL. A search of prior art records has failed to teach a method comprising the steps of;

“measuring the phase pointer activity in DC and AC components; and adjusting the phase pointer activity by compensating for the DC component of the phase pointer activity” or measuring a DC component of the phase pointer activity and repeating the step of measuring the phase pointer activity if the magnitude of the DC component is above a predetermined limit “ as disclosed in

Art Unit: 2634

claims 44 and 51, respectively. Nor does the prior art teach "comparing a received encoded character with a set predefined out-of-band (OOB) characters; and detecting an error if the encoded character is the same as any OOB character" as taught in claim 49.

*Conclusion*


12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw  
June 12, 2005

  
**CHIEH M. FAN**  
**PRIMARY EXAMINER**